Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A video stream processing circuit, ~~comprising~~comprising:

signal processing circuitry arranged to execute a first video stream processing ~~function;~~function; and

[[-]] a first and second buffer memory coupled to the signal processing circuitry for buffering the frame data produced by the first video stream processing function, the first buffer memory being coupled to the signal processing circuitry via a shareable ~~channel~~channel, the signal processing circuitry having access to the second buffer memory outside the shareable ~~channel~~channel,

[[-]] wherein the first video stream processing function comprises writing frame data of successive video frames in a temporally ordered output sequence of frames into the first and/or second buffer memory;

[[-]] the signal processing circuitry being arranged to execute a second video stream processing function using the written frame data in a temporally ordered input sequence of frames that differs from the output sequence, the second video stream processing function being arranged to select to read the frame data of predetermined first and second ones of the frames selectively from the first and second buffer memory respectively, the second ones of the frames occurring in the same temporal order in both the input and output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence.

2. (currently amended) ~~A~~ The video stream processing circuit according to Claim 1, comprising a first integrated ~~circuit~~circuit, which comprises the signal processing

circuitry and the second buffer ~~memory~~memory, and a second, separate integrated circuit that comprises the first buffer ~~memory~~memory, the shareable channel forming part of a connection between the first and second integrated circuit.

3. (currently amended) ~~A~~ The video stream processing circuit according to Claim 1, wherein the second video stream processing function is arranged to ~~last~~ read each ~~particular~~ item of frame data from the second buffer memory at respective times, the second video stream processing function being arranged to read a particular item of frame data from the second buffer memory ~~each~~ before the first video stream processing function has written a full frame following that particular item of frame data.

4. (currently amended) ~~A~~ The video stream processing circuit according to Claim 1, wherein the first video stream processing function includes an MPEG decoding function, the first ones of the frames including at least decoded MPEG P-frames, the MPEG decoding function reading frame data from decoded MPEG I-frames and decoded MPEG P frames from the first buffer memory.

5. (currently amended) ~~A~~ The video stream processing circuit according to Claim 4, wherein the second ones of the frames include B frames.

6. (currently amended) ~~A~~ The video stream processing circuit according to Claim 5, wherein the signal processing circuitry ~~the first video stream processing function~~ writes B frames to the second buffer memory only.

7. (currently amended) ~~A~~ The video stream processing circuit according to Claim 4, wherein the second ones of the frames include I frames, the first video stream processing function writing copies of the I frames to both the first and second buffer ~~memory~~memory.

8. (currently amended) ~~A~~ The video stream processing circuit according to Claim 7, wherein the second ones of the frames include B frames.

9. (currently amended) ~~A~~ The video stream processing circuit according to Claim 1, wherein the first video stream processing function comprises an MPEG decoding function, the second video stream processing function reading at least decoded MPEG P-frames from the first buffer ~~memory~~memory.

10. (currently amended) ~~A~~ The video stream processing circuit according to Claim 1, wherein the first video stream processing function, or a third video stream processing function executed by the signal processing circuitry reads only selected ones of the frames from the first buffer ~~memory~~memory, the first video processing function being arranged to write copies of the selected ones of the video frames that also are second ones of the frames to both the first and second buffer ~~memory~~memory, the first video processing function writing second ones of the frames that are not selected ones of the video frames to the second buffer memory only.

11. (currently amended) A video stream processing circuit, ~~comprising~~comprising:

[[-]] signal processing circuitry arranged to execute a first video stream processing ~~function;~~function; and

[[-]] a first and second buffer memory coupled to the signal processing circuitry for buffering the frame data produced by the first video stream processing function, the first buffer memory being coupled to the signal processing circuitry via a shareable ~~channel~~channel, the signal processing circuitry having access to the second buffer memory outside the shareable ~~channel~~channel,

[[-]] wherein the first video stream processing function comprises writing frame data of successive video frames in a temporally ordered output sequence of frames into the first and/or second buffer memory;

[[-]] the signal processing circuitry being arranged to execute a second video stream processing function using the written frame data in a temporally ordered input sequence of frames that differs from the output sequence, the first video stream processing function being arranged to select to write the frame data of predetermined first and second ones of the frames selectively to the first and second buffer memory respectively, the second ones

of the frames occurring in the same temporal order in both the input and output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence.

12. (currently amended) A method of video stream processing, the method ~~comprising~~comprising:

[[-]] using signal processing circuitry to execute a first and a second video stream processing function, the first video stream processing function producing frame data of successive video frames in a temporally ordered output sequence of frames, the second video stream processing function using the frame data in an ordered input sequence of frames that differs from the output sequence;

buffering the frame data between application of the first and second video processing function to the frame data in a first and/or second buffer memory, the first buffer memory being coupled to the signal processing circuitry via a shareable ~~channel~~channel, the signal processing circuitry not using the shareable channel to access the second buffer ~~memory~~memory; and

[[-]] reading frame data from predetermined first and second ones of the frames for use by the second video processing function selectively from the first and second buffer memory respectively, the second ones of the frames occurring in the same temporal order in both the input and output sequence, the first ones of the frames containing at least all particular frames whose position relative to the second ones of the frames in the output sequence differs from the position of the particular frames relative to the second ones of the frames in the input sequence.

13. (new) The video stream processing circuit according to Claim 1, wherein the second buffer memory has a capacity of less than one frame.

14. (new) The video stream processing circuit according to Claim 11, wherein the second buffer memory has a capacity of less than one frame.

15. (new) The method of video stream processing according to Claim 12, wherein the second buffer memory has a capacity of less than one frame.